We claim:

1. In a method of planarizing a semiconductor wafer, the improvement comprising polishing above metal interconnect lines to uniformly polish the topography of the wafer to a predetermined endpoint on the wafer sufficiently close above the metal interconnect lines, yet far enough away from said lines to prevent damage to the lines, comprising:

a) filling gaps between metal interconnect lines of an inter metal dielectric in a wafer being formed, by depositing HDP fill on top of the metal interconnects, between the metal interconnects, and on the surface of a dielectric layer between said metal interconnects to create an HDP overfill;

b) contacting the surface of HDP overfill of the processed semiconductor wafer from step a) with a fixed abrasive polishing pad; and

c) relatively moving said wafer and said fixed abrasive polishing pad to affect a polishing rate sufficient to reach a predetermined endpoint and uniformly planar surface on the wafer sufficiently close above the metal interconnect lines and yet far enough away from said lines to prevent damage to said lines.

2. The method of claim 1 wherein said metal interconnect lines are selected from the group consisting of aluminum, titanium, copper, tungsten and mixtures thereof.

3. The method of claim 2 wherein said metal interconnect lines are aluminum.

4. The method of claim 2 wherein said metal interconnect lines are titanium.

5. The method of claim 2 wherein said metal interconnect lines are copper.

6. The method of claim 2 wherein said metal interconnect lines are tungsten.

7. The method of claim 3 wherein said predetermined endpoint on the wafer is about 50nm.

8. The method of claim 4 wherein said predetermined endpoint on the wafer is about 50nm.

9. The method of claim 5 wherein said predetermined endpoint on the wafer is about 50nm.

10. The method of claim 6 wherein said predetermined endpoint on the wafer is about 50nm.

11. The method of claim 3 wherein said predetermined endpoint on the wafer is less than 50nm.

12. The method of claim 4 wherein said predetermined endpoint on the wafer is less than 50nm.

13. The method of claim 5 wherein said predetermined endpoint on the wafer is less than 50nm.

14. The method of claim 6 wherein said predetermined endpoint on the wafer is less than 50nm.

15. A semiconductor wafer produced by the method of claim 1.